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# Question Paper Code : 20392

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Seventh Semester

Electronics and Communication Engineering

EC 6009 — ADVANCED COMPUTER ARCHITECTURE

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define Instruction Set Architecture.

2. State Principle of Locality.

3. What are data hazards? List the possible data hazards in the architecture.

4. Define Branch Target Buffers.

5. The largest configuration of a Cray T90 (Cray T932) has 32 processors, each capable of generating 4 loads and 2 stores per clock cycle. The processor clock cycle is 2.167 ns, while the cycle time of the SRAMs used in the memory system is 15 ns. Calculate the minimum number of memory banks required to allow all processors to run at full memory bandwidth.

6. Draw the Structure of a vector unit containing four lanes.

7. What is Multiprocessor Cache Coherence?

8. Draw the Basic structure of a centralized shared-memory multiprocessor based on a multicore chip.

9. Write the formula to measure average memory access time for memory hierarchy performance.

10. List the Basic six Cache Optimizations for improving cache performance.

PART B — (5 × 13 = 65 marks)

11. (a) Assume a disk subsystem with the following components and MTTF :

- 10 disks, each rated at 1,000,000-hour MTTF
- 1 ATA controller, 500,000-hour MTTF
- 1 power supply, 200,000-hour MTTF
- 1 fan, 200,000-hour MTTF
- 1 ATA cable, 1,000,000-hour MTTF

Disk subsystems often have redundant power supplies to improve dependability. Using the components and MTTFs from above, calculate the reliability of redundant power supplies. Assume one power supply is sufficient to run the disk subsystem and that we are adding one redundant power supply.

Or

(b) Explain in detail about the Classes of Parallelism and Parallel Architectures.

12. (a) Explain in detail about the steps involved in Tomasulo's Algorithm with A Loop-Based examples.

Or

(b) Discuss the idea in overcoming the Data Hazards using Dynamic Scheduling.

13. (a) Explain the basic structure of a vector architecture, VMIPS and The VMIPS vector instructions, showing only the double-precision floating-point operations.

Or

(b) Explain the SIMD Instruction Set Extensions for Multimedia with an instruction category.

14. (a) Explain in detail about the State transition diagram for an individual cache block in a directory based System and the state transition diagram for the directory has the same states and structure as the transition diagram for an individual cache.

Or

(b) Discuss in detail about Snooping Coherence Protocols with an example.

15. (a) Explain the cache optimizations techniques in detail with examples.

Or

(b) Write in detail about the RAID levels in optimizations with a neat diagram.

PART C — (1 × 15 = 15 marks)

16. (a) Consider a loop like this one :

```
for (i=0;i<100; i=i+1)
{
A[i] = A[i] + B[i]; /* S1 */
B[i+1] = C[i] + D[i]; /*S2 */
}
```

Analysis the dependences between S1 and S2? Is this loop parallel? If not, show how to make it parallel.

Or

(b) Consider the following three hypothetical, but not atypical, processors, which we run with the SPEC gcc benchmark :

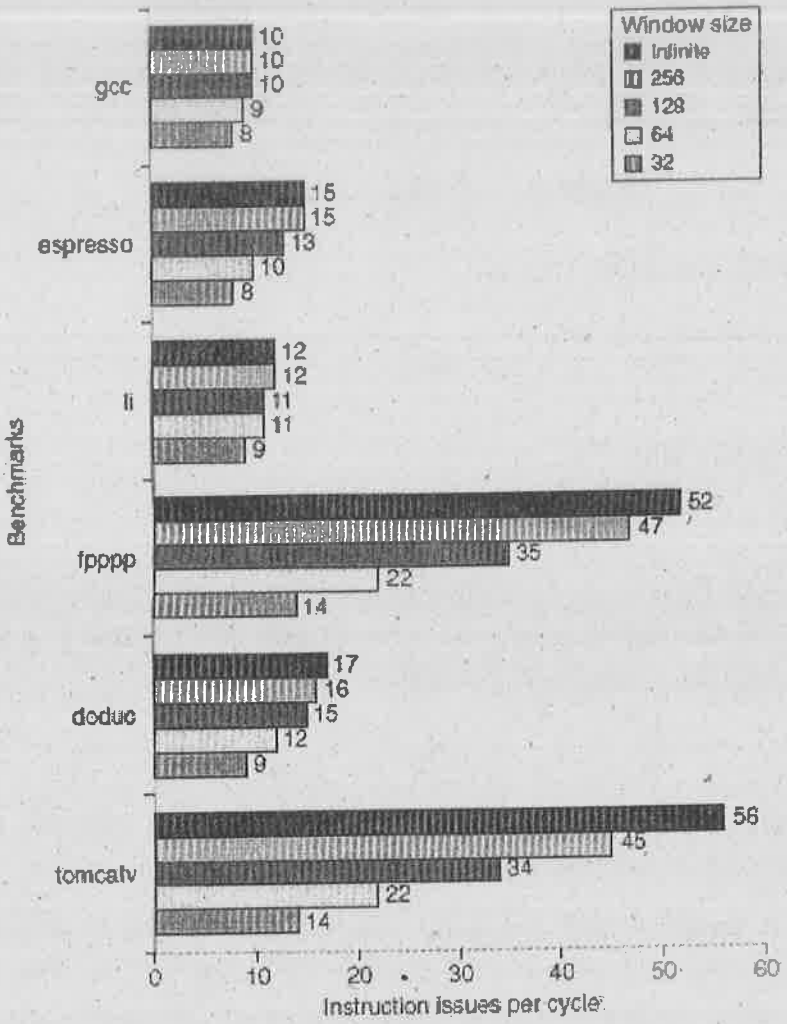
(i) A simple MIPS two-issue static pipe running at a clock rate of 4 GHz and achieving a pipeline CPI of 0.8. This processor has a cache system that yields 0.005 misses per instruction.

(ii) A deeply pipelined version of a two-issue MIPS processor with slightly smaller caches and a 5 GHz clock rate. The pipeline CPI of the processor is 1.0, and the smaller caches yield 0.0055 misses per instruction on average.

(iii) A speculative superscalar with a 64-entry window. It achieves one-half of the ideal issue rate measured for this window size. (Use the data in Figure 1.)

This processor has the smallest caches, which lead to 0.01 misses per instruction, but it hides 25% of the miss penalty on every miss by dynamic scheduling. This processor has a 2.5 GHz clock. Assume that the main memory time (which sets the miss penalty) is 50 ns. Determine the relative performance of these three processors.

Figure 1 :


Window size
Infinite
256
128
64
32
gcc
10
10
10
9
8
espresso
15
15
13
10
8
li
12
12
11
11
9
fpppp
52
47
35
22
14
doduc
17
16
15
12
9
tomcatv
56
45
34
22
14
Benchmarks
0
10
20
30
40
50
60
Instruction issues per cycle